

Claims 1-4, 6 and 7 were rejected under 35 USC 103 as being unpatentable over Quigley in view of Ziegler and further in view of Mizuno. Claim 5 was rejected as being unpatentable over the same combination further in view of Ninomiya. The rejections are respectfully traversed.

The present invention relates to a phase detector of simple construction that exhibits quick response to changes in its input signals. In one embodiment, a train of pulse-width-modulated pulses is produced. The pulses are applied to up and down current sources of a charge pump, the current sources being enabled by opposite logic levels. During a lock condition (no phase difference) of a phase lock loop, the pulses are of 50% duty cycle such that, even though both the up and down current sources are activated in sequence, the current sources negate one another and have no net effect. When a phase difference is present, one of the current sources is active for a longer time than the other current source and therefore has a predominate effect in such as way as to reduce and ultimately eliminate the phase difference.

The rejection states in part:

[I]t would have been obvious...to implement either the comparator (Fig. 8) or a RS flip-flop (38) taught by Ziegler et al. with the prior art (Figs. 2-3 of Quigley et al.) in order to prevent the non-determinate state when the two input signals (VREF, VLO) are negative-going in coincidence.

Applicant respectfully disagrees.


Quigley requires two separate regulation signals in order to control the two separate current sources of its charge pump. Ziegler requires only a single regulation signal because Ziegler teaches an all-digital implementation that does not use current sources or a charge pump but rather uses a single up-down counter.

There is no motivation found within the references themselves to attempt to modify Quigley in such a manner as to require only a single regulation signal. The motivation stated is actually a mischaracterization of the Ziegler reference. Ziegler does *not* teach preventing a non-determinate state when the two input signals (VREF, VLO) are negative-going in coincidence. Rather, Ziegler teaches that such non-determinate state is of no consequence (col. 13, lines 4-7).

Accordingly, claims 1, 4 and 7 are believed to patentably define over the cited references.

Dependent claims 2, 3, 5 and 6 are also believed to add novel and patentable subject matter to their respective independent claims. Withdrawal of the rejection and allowance of claims 1-7 is respectfully requested.

Respectfully submitted,


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